

Refine Search

Search Results -

Term	Documents
(2 AND 33).PGPB,USPT.	1
(L33 AND L2).PGPB,USPT.	1

Database:

US Pre-Grant Publication Full-Text Database
 US Patents Full-Text Database
 US OCR Full-Text Database
 EPO Abstracts Database
 JPO Abstracts Database
 Derwent World Patents Index
 IBM Technical Disclosure Bulletins

Search:

L36

Refine Search

Recall Text

Clear

Interrupt

Search History

DATE: Wednesday, May 09, 2007
 [Purge Queries](#)
 [Printable Copy](#)
 [Create Case](#)

<u>Set</u> <u>Name</u>	<u>Query</u>	<u>Hit</u> <u>Count</u>	<u>Set</u> <u>Name</u> result set
side by side			
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L36</u>	L33 and l2	1	<u>L36</u>
<u>L35</u>	L33 and l1	3	<u>L35</u>
<u>L34</u>	L33 and l7	1	<u>L34</u>
<u>L33</u>	(710/56)[CCLS]	508	<u>L33</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L32</u>	L31 and l1	2	<u>L32</u>
<u>L31</u>	toyohiko.in.	4779	<u>L31</u>
<u>L30</u>	L25 and l12	0	<u>L30</u>
<u>L29</u>	L25 and l11	0	<u>L29</u>
<u>L28</u>	L25 and l10	3	<u>L28</u>
<u>L27</u>	L25 and l9	1	<u>L27</u>

<u>L26</u>	L25 and l8	11	<u>L26</u>
<u>L25</u>	L24 and l1	198	<u>L25</u>
<u>L24</u>	L23 and (switch\$5 or select\$6 or mux\$1 or multiplex\$5 or sel) near10 (bank\$1 or section\$1 or region\$1 or area\$1)	101980	<u>L24</u>
<u>L23</u>	((conserv\$6 or reduc\$5 or minimiz\$5 or sav\$4) near7 (power or energ\$4 or consumption\$1) or sleep\$4)	1050732	<u>L23</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L22</u>	l1 and l12	1	<u>L22</u>
<u>L21</u>	l1 and l11	2	<u>L21</u>
<u>L20</u>	l1 and l10	44	<u>L20</u>
<u>L19</u>	l1 and l9	24	<u>L19</u>
<u>L18</u>	l1 and l8	130	<u>L18</u>
<u>L17</u>	l7 and l12	0	<u>L17</u>
<u>L16</u>	l7 and l11	0	<u>L16</u>
<u>L15</u>	l7 and l10	12	<u>L15</u>
<u>L14</u>	l7 and l9	3	<u>L14</u>
<u>L13</u>	l7 and l8	23	<u>L13</u>
<u>L12</u>	(713/320)[CCLS]	1534	<u>L12</u>
<u>L11</u>	(713/310-340)[CCLS]	4146	<u>L11</u>
<u>L10</u>	(711/169,173)[CCLS]	1741	<u>L10</u>
<u>L9</u>	(712/207-209,213,227)[CCLS]	2015	<u>L9</u>
<u>L8</u>	(712/2-300)[CCLS]	13320	<u>L8</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L7</u>	L1 and (switch\$5 or select\$6 or mux\$1 or multiplex\$5 or sel) near10 (bank\$1 or section\$1 or region\$1 or area\$1)	383	<u>L7</u>
<u>L6</u>	L2 and (select\$6 or mux\$1 or multiplex\$5 or sel) near10 (bank\$1 or section\$1 or region\$1 or area\$1)	22	<u>L6</u>
<u>L5</u>	L2 near45 (select\$6 or mux\$1 or multiplex\$5 or sel) near10 (bank\$1 or section\$1 or region\$1 or area\$1)	3	<u>L5</u>
<u>L4</u>	L2 near45 (select\$6 or mux\$1 or multiplex\$5 or sel) near10 (bank\$1 or section\$1 or region\$1 or area\$1)	3	<u>L4</u>
<u>L3</u>	L2 and (select\$6 or mux\$1 or multiplex\$5 or sel) near10 (bank\$1 or section\$1 or region\$1 or area\$1) near15 (reduc\$5 or minimiz\$5 or sav\$4) near7 (power or energ\$4 or consumption\$1)	2	<u>L3</u>
<u>L2</u>	L1 near15 (instruction\$1 or microinstruction\$1 or command\$1)	156	<u>L2</u>
<u>L1</u>	(fast\$2 or high\$2 or great\$2) near4 (speed or rate) near15 pipelin\$7 near15 (cach\$3 or memor\$4 or fifo\$1 or buffer\$1)	982	<u>L1</u>

END OF SEARCH HISTORY



Welcome United States Patent and Trademark Office

☐ Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

Results for "((((switch*, select*) <near/15> (bank*, region*, section*, area*, chip*) <and> (fas..."

Your search matched 23 of 3002 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

☒ e-mail

» Search Options

[View Session History](#)
[New Search](#)

» Key

IEEE JNL	IEEE Journal or Magazine
IET JNL	IET Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

Modify Search

☐ Check to search only within this results set

 Display Format: ☒ Citation ☐ Citation & Abstract

 [Select All](#) [Deselect All](#)

- ☐ **A 20 ns, low power, NMOS 1K/spl times/4 static RAM**
 Rhodes, C.; Pinkham, R.; Valente, F.; Ramsey, R.;
[Solid-State Circuits, IEEE Journal of](#)
 Volume 16, Issue 5, Oct 1981 Page(s):594 - 597
[AbstractPlus](#) | Full Text: [PDF\(808 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ **A 125-mm/sup 2/ 1-Gb NAND flash memory with 10-MByte/s program speed**
 Imamiya, K.; Nakamura, H.; Himeno, T.; Yamamura, T.; Ikehashi, T.; Takeuchi, K.; Kanda, K.; Hos-
 T.; Kawai, K.; Shiota, R.; Arai, N.; Arai, F.; Hatakeyama, K.; Hazama, H.; Saito, M.; Meguro, H.; Ch-
 Chen, J.J.;
[Solid-State Circuits, IEEE Journal of](#)
 Volume 37, Issue 11, Nov. 2002 Page(s):1493 - 1501
 Digital Object Identifier 10.1109/JSSC.2002.802355
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(849 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ **REMcode: relocating embedded code for improving system efficiency**
 Janapsatya, A.; Parameswaran, S.; Henkel, J.;
[Computers and Digital Techniques, IEE Proceedings-](#)
 Volume 151, Issue 6, 18 Nov. 2004 Page(s):457 - 465
 Digital Object Identifier 10.1049/ip-cdt:20040942
[AbstractPlus](#) | Full Text: [PDF\(552 KB\)](#) IET JNL
- ☐ **Distance associativity for high-performance energy-efficient non-uniform cache architecture**
 Chishti, Z.; Powell, M.D.; Vijaykumar, T.N.;
[Microarchitecture, 2003. MICRO-36. Proceedings. 36th Annual IEEE/ACM International Symposiur](#)
 2003 Page(s):55 - 66
 Digital Object Identifier 10.1109/MICRO.2003.1253183
[AbstractPlus](#) | Full Text: [PDF\(317 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☐ **General purpose RISC based unit: a building block for fast data acquisition systems**
 Epstein, A.; Boulin, C.;
[Real Time Conference, 1999. Santa Fe 1999. 11th IEEE NPSS](#)
 14-18 June 1999 Page(s):123 - 125
 Digital Object Identifier 10.1109/RTCON.1999.842580

[AbstractPlus](#) | Full Text: [PDF\(240 KB\)](#) IEEE CNF

[Rights and Permissions](#)

6. **Frequent loop detection using efficient nonintrusive on-chip hardware**

Gordon-Ross, A.; Vahid, F.;

[Computers, IEEE Transactions on](#)

Volume 54, Issue 10, Oct. 2005 Page(s):1203 - 1215

Digital Object Identifier 10.1109/TC.2005.165

[AbstractPlus](#) | Full Text: [PDF\(1808 KB\)](#) IEEE JNL

[Rights and Permissions](#)

7. **Functional implementation techniques for CPU cache memories**

Jih-Kwon Peir; Hsu, W.W.; Smith, A.J.;

[Computers, IEEE Transactions on](#)

Volume 48, Issue 2, Feb. 1999 Page(s):100 - 110

Digital Object Identifier 10.1109/12.752651

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(728 KB\)](#) IEEE JNL

[Rights and Permissions](#)

8. **A 9-ns HIT-delay 32-kbyte cache macro for high-speed RISC**

Nogami, K.; Sakurai, T.; Sawada, K.; Sakaue, K.; Miyazawa, Y.; Tanaka, S.; Hiruta, Y.; Kato, K.; 1
Shirotori, T.; Itoh, Y.; Uchida, M.; Iizuka, T.;

[Solid-State Circuits, IEEE Journal of](#)

Volume 25, Issue 1, Feb. 1990 Page(s):100 - 108

Digital Object Identifier 10.1109/4.50291

[AbstractPlus](#) | Full Text: [PDF\(736 KB\)](#) IEEE JNL

[Rights and Permissions](#)

9. **Networking requirements for interactive video on demand**

Nussbaumer, J.-P.; Patel, B.V.; Schaffa, F.; Sterbenz, J.P.G.;

[Selected Areas in Communications, IEEE Journal on](#)

Volume 13, Issue 5, June 1995 Page(s):779 - 787

Digital Object Identifier 10.1109/49.391753

[AbstractPlus](#) | Full Text: [PDF\(812 KB\)](#) IEEE JNL

[Rights and Permissions](#)

10. **A dynamic voltage scaled microprocessor system**

Burd, T.D.; Pering, T.A.; Stratakos, A.J.; Brodersen, R.W.;

[Solid-State Circuits, IEEE Journal of](#)

Volume 35, Issue 11, Nov. 2000 Page(s):1571 - 1580

Digital Object Identifier 10.1109/4.881202

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(200 KB\)](#) IEEE JNL

[Rights and Permissions](#)

11. **A 1.3-GOPS parallel DSP for high-performance image-processing applications**

Hinrichs, W.; Wittenburg, J.P.; Lieske, H.; Kloos, H.; Ohmacht, M.; Pirsch, P.;

[Solid-State Circuits, IEEE Journal of](#)

Volume 35, Issue 7, July 2000 Page(s):946 - 952

Digital Object Identifier 10.1109/4.848202

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(224 KB\)](#) IEEE JNL

[Rights and Permissions](#)

12. **Architectural and compiler techniques for energy reduction in high-performance microproc**

Bellas, N.; Hajj, I.N.; Polychronopoulos, C.D.; Stamoulis, G.;

[Very Large Scale Integration \(VLSI\) Systems, IEEE Transactions on](#)

Volume 8, Issue 3, June 2000 Page(s):317 - 326

Digital Object Identifier 10.1109/92.845897

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(248 KB\)](#) IEEE JNL

[Rights and Permissions](#)

13. **Reducing bandwidth requirement for delivering video over wide area networks with proxy server**
Wei-hsiu Ma; Du, D.H.C.;
[Multimedia, IEEE Transactions on](#)
Volume 4, Issue 4, Dec. 2002 Page(s):539 - 550
Digital Object Identifier 10.1109/TMM.2002.806536
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(579 KB) IEEE JNL
[Rights and Permissions](#)
14. **Adaptive vector quantization with codebook updating based on locality and history**
Guobin Shen; Bing Zeng; Liou, M.-L.;
[Image Processing, IEEE Transactions on](#)
Volume 12, Issue 3, March 2003 Page(s):283 - 295
Digital Object Identifier 10.1109/TIP.2003.810915
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(873 KB) IEEE JNL
[Rights and Permissions](#)
15. **Area-Efficient Error Protection for Caches**
Soontae Kim;
[Design, Automation and Test in Europe, 2006. DATE '06. Proceedings](#)
Volume 1, 6-10 March 2006 Page(s):1 - 6
[AbstractPlus](#) | Full Text: [PDF](#)(288 KB) IEEE CNF
[Rights and Permissions](#)
16. **A 1.3 GOPS parallel DSP for high performance image processing applications**
Hinrichs, W.; Wittenburg, J.P.; Lieske, H.; Kloos, H.; Ohmacht, M.; Kneip, J.; Ronner, K.; Pirsch, P.
[Solid-State Circuits Conference, 1999. ESSCIRC '99. Proceedings of the 25th European](#)
21-23 Sept. 1999 Page(s):102 - 105
[AbstractPlus](#) | Full Text: [PDF](#)(70 KB) IEEE CNF
[Rights and Permissions](#)
17. **Hardware Support for Prescient Instruction Prefetch**
Aamodt, T.M.; Chow, P.; Hammarlund, P.; Hong Wang; Shen, J.P.;
[High Performance Computer Architecture, 2004. HPCA-10. Proceedings. 10th International Sympo](#)
14-18 Feb. 2004 Page(s):84 - 84
Digital Object Identifier 10.1109/HPCA.2004.10028
[AbstractPlus](#) | Full Text: [PDF](#)(312 KB) IEEE CNF
[Rights and Permissions](#)
18. **Power protocol: reducing power dissipation on off-chip data buses**
Basu, K.; Choudhary, A.; Pisharath, J.; Kandemir, M.;
[Microarchitecture, 2002. \(MICRO-35\). Proceedings. 35th Annual IEEE/ACM International Symposium](#)
18-22 Nov. 2002 Page(s):345 - 355
Digital Object Identifier 10.1109/MICRO.2002.1176262
[AbstractPlus](#) | Full Text: [PDF](#)(467 KB) IEEE CNF
[Rights and Permissions](#)
19. **Non-vital loads**
Rakvic, T.; Black, T.; Limaye, D.; Shen, T.P.;
[High-Performance Computer Architecture, 2002. Proceedings. Eighth International Symposium on](#)
2-6 Feb. 2002 Page(s):165 - 174
[AbstractPlus](#) | Full Text: [PDF](#)(286 KB) IEEE CNF
[Rights and Permissions](#)
20. **Cache decay: exploiting generational behavior to reduce cache leakage power**
Kaxiras, S.; Zhigang Hu; Martonosi, M.;
[Computer Architecture, 2001. Proceedings. 28th Annual International Symposium on](#)
30 June-4 July 2001 Page(s):240 - 251

Digital Object Identifier 10.1109/ISCA.2001.937453

[AbstractPlus](#) | Full Text: [PDF](#)(380 KB) IEEE CNF

[Rights and Permissions](#)



21. Reducing bandwidth requirement for delivering video over wide area networks with proxy s

Wei-Hsiu Ma; Du, D.H.C.;

[Multimedia and Expo, 2000, ICME 2000, 2000 IEEE International Conference on](#)
Volume 2, 30 July-2 Aug. 2000 Page(s):991 - 994 vol.2

Digital Object Identifier 10.1109/ICME.2000.871526

[AbstractPlus](#) | Full Text: [PDF](#)(432 KB) IEEE CNF

[Rights and Permissions](#)



22. On-chip cache memory resilience

Hwang, S.H.; Choi, G.S.;

[High-Assurance Systems Engineering Symposium, 1998, Proceedings, Third IEEE International](#)
13-14 Nov. 1998 Page(s):240 - 247

Digital Object Identifier 10.1109/HASE.1998.731620

[AbstractPlus](#) | Full Text: [PDF](#)(80 KB) IEEE CNF

[Rights and Permissions](#)



23. A 400 MHz 4.5 Mb synchronous BICMOS SRAM with alternating bit-line loads

Suzuki, A.; Kobayashi, T.; Hamano, T.; Hatada, H.; Kawasumi, A.; Matsuoka, F.; Ishimaru, K.; Tak
M.; Okayama, Y.; Unno, Y.; Kakumu, M.; Tsujimoto, J.;

[Solid-State Circuits Conference, 1996, Digest of Technical Papers, 43rd ISSCC., 1996 IEEE Intern](#)
8-10 Feb. 1996 Page(s):146 - 147, 433

Digital Object Identifier 10.1109/ISSCC.1996.488546

[AbstractPlus](#) | Full Text: [PDF](#)(1128 KB) IEEE CNF

[Rights and Permissions](#)

[Help](#) [Contact Us](#) [Privac](#)

© Copyright 2006 IE

Indexed by
 Inspec®